We claim:

1. A method of controlling and monitoring the thickness variation of a film structure of a semiconductor wafer, said semiconductor wafer including at least one device region and a testing region, said device region and said testing region having the same film structure, said testing region is utilized, in a CMP process, to control and monitor the thickness variation of said film structure of said device region, said method comprising:

calculating a first pattern density of said film structure of said device region;

etching said film structure of said testing region that a second pattern density of said film structure of said testing region being substantially compatible with said first pattern density of said device region; and

polishing said semiconductor wafer and monitoring the thickness variation of said film structure of said testing region.

2. The method as recited in claim 1, wherein said second pattern density of said testing region is less than 10 times said first pattern density of said device region.

3. The method as recited in claim 1, wherein said second pattern density of said testing region is exactly the same with said first pattern density of said device region.

4. The method as recited in claim 1, further comprises to form a plurality of shallow trenches within the substrate of said device region, while said testing region having a planar surface.

5. The method as recited in claim 1, wherein said film structure further comprises a first dielectric layer and a second dielectric layer on said first dielectric layer, partially removing said second dielectric layer on said device region and forming a plurality of the second dielectric blocks to cover said shallow trenches, the size of each of the second dielectric blocks is substantially the same.

6. The method as recited in claim 5, wherein said first pattern density of said film structure of said device region is obtained by calculating a ratio of the area of the second dielectric blocks to the total area of said device region.

7. The method as recited in claim 5, wherein said first dielectric layer further comprises a silicon nitride layer as a stop layer in a CMP process.

8. The method as recited in claim 5, further utilizes a high density plasma CVD to form a silicon oxide layer as said second dielectric layer.

9. A planarization method of a semiconductor wafer, with a plurality of shallow trenches, said semiconductor having at least one device region and a testing region, said device region having said shallow trenches and said

testing region having a planar surface, said device region and said testing region having a film structure, said film structure at least having a first dielectric layer and a second dielectric layer on said first dielectric layer, said testing region is utilized, in a CMP process, to control and monitor the thickness variation of said film structure of said device region, said method comprising:

removing a portion of said second dielectric layer on said device region and forming a plurality of the second dielectric blocks;

calculating a first pattern density of said film structure of said device region;

etching said film structure of said testing region that a second pattern density of said film structure of said testing region being substantially compatible with said first pattern density of said device region; and

polishing said semiconductor wafer and monitoring the thickness variation of said film structure of said testing region.

10. The method as recited in claim 9, wherein said second pattern density of said testing region is less than 10 times said first pattern density of said device region.

11. The method as recited in claim 9, wherein said second pattern density of said testing region is exactly the same with said first pattern density of said device region.

12. The method as recited in claim 9, wherein said second dielectric blocks cover said shallow trenches and the size of each of the second dielectric blocks is substantially the same.

13. The method as recited in claim 9, wherein said first pattern density of said film structure of said device region is obtained by calculating a ratio of the area of the second dielectric blocks to the total area of said device region.

14. The method as recited in claim 9, wherein said first dielectric layer further comprises a silicon nitride layer as a stop layer in a CMP process.

15. The method as recited in claim 9, further utilizes a high density plasma CVD to form a silicon oxide layer as said second dielectric layer.